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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/058,264	01/29/2002	Koji Tomioka	NEC01P260-HYa	4190

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EXAMINER	
MARTIN, CIARA A	
ART UNIT	PAPER NUMBER
2157	

DATE MAILED: 01/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/058,264	TOMIOKA, KOJI	
	Examiner	Art Unit	
	Ciara Martin	2157	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/29/02; 11/22/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the application filed on January 29, 2002. Claims 1-17 are pending. Claims 1-17 represent a computer system, CPU and memory installed apparatus, and input/output control apparatus.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Adelman et al. US 6006259 A.

As per claim 1, Adelman teaches a clustered computer system comprising a plurality of CPU and memory installed apparatus each having at least one CPU and at least one memory (4:33-48), and a plurality of input/output control apparatus (4:33-48), said CPU and memory installed apparatus and said input/output control apparatus being connected to each other by a network (3:66-4:48, claims 1 and 8).

As per claim 2, Adelman teaches a computer system comprising a plurality of CPU and memory installed apparatus each having at least one CPU and at least one memory, a plurality of input/output control apparatus, and a network connecting said CPU and memory installed apparatus and said input/output control apparatus to each other (4:14-48), each of said CPU and memory installed apparatus having communication means for transmitting an input/output instruction issued by said CPU of

an own CPU and memory installed apparatus to said input/output control apparatus assigned in advance to the own CPU and memory installed apparatus via said network (4:33-48, 5:20-41), and receiving a response from said input/output control apparatus via said network (4:33-48), and each of said input/output control apparatus having communication means for receiving an input/output instruction from said CPU and memory installed apparatus assigned in advance to an own input/output control apparatus via said network (4:33-48), and transmitting a response to said input/output instruction to said CPU and memory installed apparatus via said network (3:66-4:48, claims 1 and 8).

As per claim 3, Adelman teaches a computer system according to claim 2, wherein said communication means of each of said input/output control apparatus comprises means for receiving an input/output instruction as being effective only when the source of the input/output instruction received via said network is a CPU and memory installed apparatus which has been set in advance (3:66-4:48).

As per claim 4, Adelman teaches a computer system according to claim 2, wherein said communication means of each of said CPU and memory installed apparatus comprises means for receiving a response as being effective only when the source of the response received via said network is an input/output control apparatus which has been set in advance (3:66-4:48).

As per claim 5, Adelman teaches a computer system according to claim 2, wherein said network is also used for communications between said plurality of CPU and memory installed apparatus (3:66-4:48).

As per claim 6, Adelman teaches a computer system according to claim 3, wherein said communication means of each of said CPU and memory installed apparatus comprises means for receiving a response as being effective only when the source of the response received via said network is an input/output control apparatus which has been set in advance (3:66-4:48).

As per claim 7, Adelman teaches a computer system according to claim 5, wherein said communication means of each of said CPU and memory installed apparatus comprises means for communicating with other CPU and memory installed apparatus via said network (3:66-4:48).

As per claim 8, Adelman teaches a computer system according to claim 7, wherein the communications between said plurality of CPU and memory installed apparatus are communications for accessing memories installed on other CPU and memory installed apparatus (3:66-4:48).

As per claim 9, Adelman teaches a computer system according to claim 2, further comprising means for, when either one of said CPU and memory installed apparatus fails to operate due to a fault, assigning said input/output control apparatus which has been used by the faulty CPU and memory installed apparatus to another normal CPU and memory installed apparatus hereby to continue system operation (4:66-5:19, 12:12-34

As per claim 10, Adelman teaches a computer system according to claim 9, wherein an active one of the CPU and memory installed apparatus which is using

another input/output control apparatus is used as said other normal CPU and memory installed apparatus (4:66-5:19).

As per claim 11, Adelman teaches a computer system according to claim 9, further comprising a backup CPU and memory installed apparatus, said backup CPU and memory installed apparatus being used as said other normal CPU and memory installed apparatus (4:66-5:19).

As per claim 12, Adelman teaches a computer system according to claim 2, further comprising at least one backup input/output control apparatus, and means for, when either active one of said input/output control apparatus fails to operate due to a fault, assigning said backup input/output control apparatus to said CPU and memory installed apparatus which has been using the faulty input/output control apparatus thereby to continue system operation (4:66-5:19).

As per claim 13, Adelman teaches a computer system comprising a CPU and memory installed apparatus having at least one CPU and at least one memory, an input/output control apparatus, and a communication cable connecting said CPU and memory installed apparatus and said input/output control apparatus to each other, said CPU and memory installed apparatus having communication means for transmitting an input/output instruction issued by said CPU to said input/output control apparatus via said communication cable, and receiving a response from said input/output control apparatus via said communication cable, and said input/output control apparatus having communication means for receiving an input/output instruction from said CPU and memory installed apparatus via said communication cable, and transmitting a response

to said input/output instruction to said CPU and memory installed apparatus via said communication cable (4:14-33).

As per claim 14, Adelman teaches a CPU and memory installed apparatus comprising at least one CPU and at least one memory, communication means for communicating with an external circuit, transmitting an input/output instruction issued by said CPU to an input/output control apparatus which has been assigned in advance, and receiving a response from said input/output control apparatus, and a single board on which said CPU, said memory, and said communication means are mounted (4:13-48).

As per claim 15, Adelman teaches a CPU and memory installed apparatus according to claim 14, wherein said communication means has means for receiving said response as being effective only when the source of the received response is the input/output control apparatus which has been assigned in advance (4:33-48).

As per claim 16, Adelman teaches an input/output control apparatus comprising an input/output control circuit for controlling a peripheral device based on an input/output instruction, communication means for communicating with an external circuit, receiving an input/output instruction from a CPU and memory installed apparatus which has been set in advance and transferring said input/output instruction to said input/output control circuit, and transmitting a response to said input/output instruction to said CPU and memory installed apparatus (9:21-49)

As per claim 17, Adelman teaches an input/output control apparatus according to claim 16, wherein said communication means has means for receiving said input/output

instruction as being effective only when the source of the received input/output instruction is the CPU and memory installed apparatus which has been set in advance (9:21-49).

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ciara Martin whose telephone number is 571-272-7507. The examiner can normally be reached on M-F 6:30- 4:00 with second Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ario Etienne can be reached on 571-272-4001. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CM
1/18/06

ARIO ETIENNE
PRIMARY EXAMINER